Serial No.: 10/826,198
Group Art Unit: 2634

REMARKS

Response to Arguments

Drawings

The Examiner stated that the drawings are objected to because written labels for components of the invention are needed to clarify the drawings. The Examiner stated that, for example, 218 should have a written term "Dither Unit" along with the numerical number.

It is noted that the objection to the drawings is a verbatim repetition of the prior objection, with no further explanation and no response or reply to the Applicant's traversal and the Applicant's arguments with respect thereto.

The objection to the drawings is again traversed.

As a first ground of traversal, the Examiner offered no explanation – either in the present or in the prior Office Action – concerning the alleged inadequacy in the drawings. On the other hand, the Applicant's response explained that the principle elements represented in the drawings are all readily understandable by those having ordinary skill in the art by reference to the Applicant's detailed description without the need for legends or labeled textual descriptions in the drawings.

It is additionally pointed out that blocks are universal symbols for modules, circuits, and components, and that it is well established that modules, circuits, and components are not supposed to be labeled.

Thus, the network 112, represented by a figurative "cloud", is a common and readily recognized symbol for the Internet. The transmission channels 108, represented by open arrows, are common and readily recognized symbols for transmission channels. The transmitter 110, connected to the base of a transmission channel arrow 108, is readily understandable, by confirmatory reference thereto in the specification, as a transmitter. The receiver 106, connected to the head of a transmission channel arrow 108, is readily understandable, by confirmatory reference thereto in the specification, as a receiver. And so forth for the remaining elements of the invention equally clearly identified, recognizable, and understandable, as described, by a person having ordinary skill in the art.

With regard to the repeated drawings objection in the present Office Action, as noted, the Examiner did not explain why the Applicant's explanation was not accepted, nor otherwise clarify the basis of the objection. Rather, the prior objection was merely repeated verbatim. Such an unexplained and unclarified objection to the drawings cannot be maintained because it is well established that the Applicant cannot be made to guess the reasons behind and the basis of an Examiner's objection. This was made clear in *Ex parte* Schricker:

> "The examiner has left applicant and the board to guess at the basis of the rejection and after having us guess would have us figure out (i.e., further guess) what part of which [prior art] document supports the rejection. We are not good at guessing; hence, we decline to guess." *Ex parte* Schricker, 56 USPQ2d 1723 (B.P.A.I. 2000) (unpublished).

The policy requiring such full explanation by the Examiner is recognized in MPEP §707.07(f), which requires that:

> "Where the applicant traverses any rejection, the examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it."

Additionally, the Applicant pointed out that the Examiner's objections were inconsistent with the requirements expressly set forth under 37 CFR §1.74, which specifies that "...the detailed description of the invention shall refer...to the different parts by use of reference letters or numerals (preferably the latter)." The drawings that have been objected to are clearly in complete conformity with the requirements of 37 CFR §1.74. But in maintaining the objection, no explanation or reconciliation was given by the Examiner concerning the requirements under 37 CFR §1.74 that directly contradict the Examiner's objection to the drawings. Therefore, the Applicant has again been left to guess the basis for the drawings objections. This too is improper and cannot be sustained because of *Ex parte* Schricker and MPEP §707.07(f), *supra*.

Another concern and consideration is that the requirement for labeled representations will place undue expense and burden on the Applicant not only in the present application, but as well in any corresponding foreign applications in which the drawings would have to be counter-edited to meet local foreign requirements, if not as well the additional and unnecessary expense to conform to PCT requirements.

Finally, it was also pointed out in the prior response that the USPTO is a PCT receiving office and is bound by PCT Rule 11.11, which states that "...drawings shall not contain text matter, except a single word or words, when absolutely indispensable...". Since the Examiner has not shown or explained why such textual matter is not *absolutely indispensable* in the present drawings, the drawing objections need to be withdrawn in order to be in compliance with controlling PCT Rule 11.11.

For all these reasons, such withdrawal is earnestly and respectfully requested.

Claim Rejections and Objections

The Examiner stated that the Applicant's arguments filed July 25, 2005, have been fully considered but are not considered persuasive for claims 1, 2, 4, 6, 7, 9–17, 19, and 20. Accordingly, clarifications have been made in the Applicant's responding remarks below, with a view to facilitating a clearer understanding of the Applicant's position with respect thereto. In addition, independent claims 1, 6, 11, and 16 have been clarified to amend the previously claimed combinations, as also addressed below. The support for these amendments is on page 8, line 25, and on page 15, lines 4–6.

Claim Rejections - 35 USC §103

Claims 1 and 4 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa").

Kelkar provides an integrated circuit chip having built-in self-measurement for phase lock loop output clock jitter and phase error. An edge sorting circuit measures jitter between corresponding transition edges of a measured clock and a reference clock. A decoder circuit reads in the value and increments a corresponding counter. A state machine then reads the counters, processes the information, and outputs one or more PLL clock error values.

Yanagisawa provides a phase difference detector for detecting a phase difference between two input signals, and a jitter detector and method for detecting the amount of jitter between the two input signals. The jitter detector obtains a digital phase difference value

between the two input signals. A comparison pulse generator outputs a series of phase difference comparison pulses. A periodic signal generator outputs a periodic signal every time a value obtained by accumulating the widths of the phase difference comparison pulses exceeds a predetermined value. A counter counts the number of pulses of the clock signal and an arithmetic unit detects and outputs a variation in the count as jitter between the first and second input signals.

The independent claims 1, 6, 11, and 16 have been clarified to amend the previously claimed combination, as exemplified in claim 1, to now include the limitations that the jitter that is being measured is jitter on a data signal, and that the invention is digital, not analog:

> "A method for measuring jitter on a data signal, comprising:
> inputting a data signal under test to digitally generate data signal transition locations;
> digitally latching a data signal transition location using a sampling clock signal;
> digitally converting the data signal transition location to a delay value;
> digitally converting the delay value to an edge position output; and
> digitally detecting a value of the edge position output."

Regarding claim 1, the Applicant respectfully traverses the rejection on the grounds that the Applicant's claimed combination would be patentable over Kelkar in view of Yanagisawa since the Applicants' claimed combination now includes the limitations not disclosed in Kelkar of:

> "A method for measuring jitter on a <u>data</u> signal, comprising:
> inputting a <u>data</u> signal under test to digitally generate <u>data</u> signal transition locations;
> digitally latching a <u>data</u> signal transition location using a sampling clock signal;
> digitally converting the <u>data</u> signal transition location to a delay value;
> digitally converting the delay value to an edge position output; and
> digitally detecting a value of the edge position output." [underlining for clarity]

The Examiner states in the Office Action dated October 5, 2005:

> "an inputting signal"

However, Kelkar does not teach or suggest measuring jitter on a data signal, as now claimed, but at column 3, lines 19–23, teaches:

> "FIG. 1 depicts a high level block diagram 10 showing the components of a system that measures the PLL timing error between a reference clock (e.g., the input to a PLL) and a measured clock (i.e., the output of a PLL)." [underlining for clarity]

The "measured clock" (the continuously running output of the PLL) is not a data signal but is a continuously running clock signal. The Kelkar patent describes a system for measuring the jitter present on a clock signal. It does not describe measurement of jitter on a data signal. For example, in column 4, lines 46–53, there is a table demonstrating the output value corresponding to time delay. Notably, if the input measurement signal is a data signal and not a clock, the output value will take the value of "0000" or "1111" in any bit period where there is no transition. Kelkar does not teach or disclose how to manage this situation, and therefore cannot measure jitter on a data signal, as now claimed.

The above shows that Kelkar does not teach or suggest measuring jitter on a data signal, and shows that Kelkar would in fact be inoperative for a data signal measurement.

Accordingly, and based upon the above, it is respectfully submitted that claim 1, as well as claims 2–5 dependant thereon, are allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because, when the combination would produce an inoperative device, the combination cannot be obvious according to the CAFC:

> "If references taken in combination would produce a "seemingly inoperative device", we have held that such references teach away from the combination and thus cannot serve as predicates for a prima facia case of obviousness." *In re* Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)

The Applicant also respectfully traverses the rejection of claim 1 on the grounds that the Applicant's claimed combination would be patentable over Kelkar in view of Yanagisawa since the Applicants' claimed combination now includes the limitations not disclosed in Kelkar of:

"A method for measuring jitter on a data signal, comprising:

> inputting a data signal under test to digitally generate data signal transition locations;
> digitally latching a data signal transition location using a sampling clock signal;
> digitally converting the data signal transition location to a delay value;
> digitally converting the delay value to an edge position output; and
> digitally detecting a value of the edge position output." [underlining for clarity]

The Examiner states in the Office Action dated October 5, 2005:

> "...latching or sorting the transition location using a sampling clock signal (Col. 3, lines 42-44), converting the signal transition to a delay value (Col. 3, 45-53)"

However, Kelkar does not teach or suggest digitally latching and converting, as now claimed, but at column 5, line 66 – column 6, line 2, while describing Fig. 5, teaches:

> "The phase detector output controls a charge pump 90 that charges or discharges a loop filter capacitor 86, which provides the delay control signal 85 to the variable delay line 83." [underlining for clarity]

Thus, Kelkar teaches an analog delay locked loop for the variable delay line (Fig. 5) that is required in Kelkar's device. In contrast, the present invention, as now claimed, is digital, not analog. In fact, the present invention does not even require a variable delay line, as taught by Kelkar, because the present invention uses its own calibrator to accommodate anomalous physical delay variations in the delay elements. This obviates the need for the analog delay locked loop taught in Fig. 5 of Kelkar.

Accordingly, and based upon the above, it is respectfully submitted that claim 1, as well as claims 2–5 dependant thereon, are allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because Kelkar's analog delay locked loop teaches away from the present invention:

> "We have noted elsewhere, as a "useful general rule," that references that teach away cannot serve to create a prima facie case of obviousness." *In re* Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984)

In fact, it is additionally clear that one of ordinary skill in the art would not look to Kelkar for teachings relevant to the present invention, even in hindsight. Thus, Kelkar provides no motivation for a person of ordinary skill in the art to attempt the suggested

combination. For example, Kelkar describes a delay line in which only the entire delay line has a known delay. Kelkar assumes this total delay is evenly shared throughout the delay elements within the delay line. One of ordinary skill in the art would readily recognize that this cannot be assumed to be the case. In contrast, the present invention separately calibrates each and every delay element individually. Further, Kelkar uses a set of N counters to measure what is effectively the jitter probability density function. Although perhaps useful in PLL characterization, this is not generally a useful measurement in the communications area unless the jitter signal has been filtered first. See, for example, ITU-T O.171/O.172. In contrast, the present invention uses the data from the tapped delay line to process not only the peak-to-peak value of the jitter, but also the spectral content.

Not only is it thus clear that one of ordinary skill in the art would not look to Kelkar for teachings relevant to the present invention, but in addition, the Examiner has not shown or cited a specific section in Kelkar that would support the Examiner's statement that:

> "It would be obvious to one skilled in the art to combine Kelkar et al's invention with Yanagisawa et al to produce multiple delays of the input signal to make the jitter between the signals easily detectable. (Abstract of Yanagisawa et al, lines 2-3)"

But Yanagisawa's Abstract, lines 1–3, merely states:

> "A jitter detector obtains a phase difference between input signals as a digital value to make jitter between the signals easily detectable."

Thus, no motivation has been cited or presented in either Kelkar or Yanagisawa for a person of ordinary skill in the art to attempt the suggested combination. It is not sufficient that the proposed combination, if feasible, might be beneficial. Rather, it is necessary, as explained in *In re* Sang-Su Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), that there be a specific suggestion in one of the references to make the combination. In *In re* Sang-Su Lee, the Court held that the conclusion of obviousness may not be made from common knowledge and common sense of a person of ordinary skill in the art without any *specific* hint or suggestion in a particular reference.

In *In re* Sang-Su Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), the application was directed to a method of automatically displaying functions of a video display device and demonstrating how to select and adjust the function in order to facilitate response

by the user. The examiner rejection was based on obviousness based on two references. One reference was for a television menu for adjusting the picture and audio functions without a demonstration of how to adjust the functions. The other reference was for a videogame having a demonstration mode without showing adjusting the picture or audio functions. The Examiner's rationale for the combination was that it:

> "would have been obvious to one of ordinary skill in the art since the demonstration mode is just a programmable feature which can be used in many different device(s) for providing automatic introduction by adding the proper programming software," and that "another motivation would be that the automatic demonstration mode is user friendly and it functions as a tutorial."

On appeal to the Board, the Board upheld the rejection by stating:

> "The conclusion of obviousness may be made from common knowledge and common sense of a person of ordinary skill in the art without any specific hint or suggestion in a particular reference."

The CAFC vacated and remanded stating in particular that the Board's rejection of the need "for any specific hint or suggestion in a particular reference" to support the combination of the references was an "[o]mission of a relevant factor required by precedent [which] is both legal error and arbitrary agency action." [insertion and underlining for clarity]

Therefore, inasmuch as the Examiner has not cited in either Kelkar or Yanagisawa any such specific hint or suggestion for the combination, the rejection based upon the assumed benefits of the hypothetical combination of Kelkar in view of Yanagisawa cannot be maintained, and independent claim 1 is accordingly believed to be allowable thereover on this ground as well. Allowance thereof is therefore respectfully requested.

With regard to Yanagisawa, the Applicant also respectfully traverses the rejection of claim 1 on the grounds that the Applicant's claimed combination would be patentable over Kelkar in view of Yanagisawa since the Applicants' claimed combination now includes the limitations not disclosed in Kelkar of:

> "A method for measuring jitter on a data signal, comprising:
> inputting a data signal under test to digitally generate data signal transition locations;
> digitally latching a data signal transition location using a sampling clock signal;
> digitally converting the data signal transition location to a delay value;

> digitally converting the delay value to an edge position output; and
> digitally detecting a value of the edge position output." [underlining for clarity]

The Examiner states in the Office Action dated October 5, 2005:

> "Yanagisawa et al discloses an edge detector converts the first and second signal into first and second timing signals, a comparison pulse generator that outputs the phase difference or delay value of the first and second timing signals. (Fig. 7, labels 107 and 103)"

However, Yanagisawa also employs analog circuitry, as taught at column 6, lines 24–33:

> "...the phase difference is converted into a charge quantity.
> The capacitor 10431 sequentially stores this charge. The voltage of the capacitor 10431, i.e., a potential level at a node 10433, is variable with the quantity of the charge that has been stored on the capacitor 10431. In other words, the potential level at the node 10433 is determined depending on the capacitance value of the capacitor 10431 and the cumulative phase difference between the first and second input signals 101 and 102." [underlining for clarity]

Therefore, for the same reasons that one of ordinary skill in the art would not look to Kelkar for teachings relevant to the digital implementation of present invention, one of ordinary skill in the art would likewise not look to Yanagisawa. This therefore provides additional reasons why there is no motivation to combine these references.

For example, the jitter measurement in Yanagisawa uses a current source charging a capacitor, as indicated above. A comparator measures when the voltage on the capacitor reaches a given level. This may take several cycles of the signal to be measured. The time for this to happen is measured by a counter that counts clock edges and is reset at the start of the measurement and counts until the end of the measurement. One of ordinary skill in the art considering the digital teachings of the present invention would therefore not look to Yanagisawa because, *inter alia*:

- The present invention measures jitter on a data signal that can have any digital content. The present invention does not require a guaranteed transition for every bit period / unit interval (UI).

- The present invention gives a jitter measurement on every transition of the input signal to be measured. Yanagisawa potentially requires a lot of transitions, particularly if the phases of the input signals are very similar. This means the present invention can measure higher frequency jitter, as the bandwidth of the jitter that can be measure is limited by the Nyquist frequency, i.e. half the sample rate. Yanagisawa's sample rate can be slow if a lot of cycles are needed to take a measurement.

- The present invention's measurement is purely digital with no analog circuitry. It does not require a current that is charging a capacitor, and therefore does not suffer from noise on the capacitor signals or charge current or current source and capacitor manufacturing tolerances. If the capacitor is a ±10% device, the timing accuracy it can achieve is ±10% within a batch of products. If the current from the current source is not as designed due to manufacturing variances, the accuracy is affected.

- The present invention does not require a comparator. Any noise on either of the comparator inputs in Yanagisawa can cause inaccuracy in the timing measurement. This is particularly acute if the phase difference between the two inputs (101 and 102 in Yanagisawa) is small. The voltage on the capacitor (10433 in Fig. 5 of Yanagisawa) will increase very slowly, thereby leading to large inaccuracies of measurement if any noise is present. Also, the comparator must be manufactured to have an accurate offset voltage.

- The resolution of Yanagisawa is limited by the speed that the counter can clock. The present invention is not limited by this, but by the delay of a single delay element. In any given digital technology, the present invention will therefore have superior resolution. In the case of an FPGA implementation of the present invention with current technologies, this is potentially as much as 80 times the resolution of the Yanagisawa teachings.

Thus, as indicated, one of ordinary skill in the art would not look to Yanagisawa for teachings relevant to the digital implementation of present invention, and there would therefore be no motivation to combine Yanagisawa with Kelkar.

Accordingly, and based upon the above, it is respectfully submitted that claim 1, as well as claims 2–5 dependant thereon, are allowable under 35 U.S.C. §103(a) as being unobvious over Kelkar in view of Yanagisawa to a person having ordinary skill in the art at the time the invention was made.

Regarding claim 4, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth therein and additionally claims non-obvious combinations thereof.

The Applicant also respectfully traverses the rejection of claim 4 on the grounds that the Applicant's claimed combination would be patentable over Kelkar in view of Yanagisawa since the Applicant's claimed combination includes the limitation not disclosed in Yanagisawa of:

> "analyzing the edge position output to determine edge position movement in excess of a predetermined magnitude." [underlining for clarity]

The Examiner states in the Office Action:

> "Yanagisawa et al discloses a comparator comparing the phase different or edge movement exceeding a predetermined value. (Abstract, lines 9-12)"

However, Yanagisawa does not show determining edge position movement in excess of a predetermined magnitude because Yanagisawa, Abstract, lines 8-12, states:

> "The periodic signal generator outputs a periodic signal every time a value obtained by accumulating the widths of the phase difference comparison pulses exceeds a predetermined value." [underlining for clarity]

The above shows that Yanagisawa is accumulating multiple values, and thus neither describes nor suggests analyzing the edge position output to determine edge position movement in excess of a predetermined magnitude, as called for in claim 4.

Accordingly, and based upon the above, it is respectfully submitted that claim 4 is allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because:

> "[T]he prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be

found in the prior art, and not based on applicant's disclosure." *In re* Vaeck, 947 F2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

Allowance of claim 4 is therefore respectfully requested on this ground as well because of *In re* Gordon, *In re* Sang-Su Lee, and *In re* Vaeck *supra*.

Claims 2, 6-7, 9-12, and 14-15 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa"), and further in view of Sunter et al. (US Application No.: 2005/0069031, hereinafter "Sunter").

Kelkar and Yanagisawa were previously summarized above.

Sunter measures a statistical value of jitter for a data signal. The data signal is digitally sampled to produce sampled logic values, and the sampled values are analyzed to deduce a statistical value of the jitter.

Regarding claims 2, 7, 9, 10, 12, 14, and 15, the Applicant respectfully traverses the rejection because the rejection was merely presented again verbatim with no new grounds of rejection being presented and no explanation or rebuttal provided concerning the Applicants' prior response regarding claims 2, 7, 9, 10, 12, 14, and 15. The Examiner's statement that "the rejection still stands due to the rejection of the independent claim [1, 6, 11]" is clearly inappropriate in view of MPEP §707.07(f) and *Ex parte* Schricker, *supra*, and by failing to rebut the Applicant's traversal, the Examiner has failed to establish a *prima facie* case for an obviousness rejection:

> "When the references cited by the Examiner fail to establish a *prima facie* case of obviousness, the rejection is improper and will be overturned." (*In re* Fine, 837 Fed. 2d 1071, 1074, 5 USPQ 2d 1596, 1598 (Fed. Cir. 1988)).

Having presented a rebuttal to the Examiner's rejection, the burden is not on the Applicant to provide evidence at this stage, but rather on the Examiner, because:

> "It is by now well settled that the burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office." *Ex parte* Skinner, 2 USPQ2d 1788, 1788-89 (B.P.A.I. 1986).

> "As adapted to ex parte procedure, Graham [v. John Deere Co.] is interpreted as continuing to place the 'burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103.'" *In re* Piasecki, 745 F.2d 1468, 223 USPQ 785, 788 (Fed. Cir. 1984), quoting *In re* Warner, 379 F.2d 1011, 154 USPQ 173, 177 (C.C.P.A. 1967), *cert. denied*, 389 U.S. 1057 (1968). [underlining for clarity]

Since the Examiner has produced no such factual basis, withdrawal of this rejection and allowance of claims 2, 7, 9, 10, 12, 14, and 15 is respectfully requested.

With regard to the repeated rejection of claims 6 and 11, these same issues have been discussed in detail above with respect to the rejection of claim 1, and those arguments are equally applicable to the rejection of claims 6 and 11. Consequently, the Applicants' claimed combination would be patentable over Kelkar in view of Yanagisawa and further in view of Sunter. On those same bases, therefore, the Applicants respectfully traverse the rejection of claims 6 and 11.

Accordingly, and based on the above, since there is no teaching or motivation in these references for the hypothetical combination of Kelkar in view of Yanagisawa and further in view of Sunter, as suggested by the Examiner, it is respectfully submitted that claims 6 and 11 are allowable under 35 USC §103 as being unobvious at the time the invention was made to a person having ordinary skill in the art. *In re* Gordon, *In re* Sang-Su Lee, *In re* Vaeck, *In re* Fine, *Ex parte* Skinner, *In re* Piasecki, and *In re* Warner, quoted above.

Claims 16-17, and 19-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa"), further in view of Sunter et al. (US Application No.: 2005/0069031, hereinafter "Sunter"), and further in view of IEEE Design and Test of Computers, ("FPGA and CPLD Architectures: A Tutorial", hereinafter "IEEE").

Kelkar, Yanagisawa, and Sunter were previously summarized above.

IEEE provides a tutorial on FPGA and CPLD architectures.

With regard to the repeated rejection of claim 16, these same issues have been discussed in detail above with respect to the rejections of claims 1, 6, and 11, and those arguments are equally applicable to the rejection of claim 16. Consequently, the Applicants' claimed combination would be patentable over Kelkar in view of Yanagisawa, further in view of Sunter, and further in view of IEEE. On those same bases, therefore, the Applicants respectfully traverse the rejection of claim 16.

Accordingly, and based on the above, since there is no teaching or motivation in these references for the hypothetical combination of Kelkar in view of Yanagisawa, further in view of Sunter, and further in view of IEEE, as suggested by the Examiner, it is respectfully submitted that claim 16 is allowable under 35 USC §103 as being unobvious at the time the invention was made to a person having ordinary skill in the art. *In re* Gordon, *In re* Sang-Su Lee, *In re* Vaeck, *In re* Fine, *Ex parte* Skinner, *In re* Piasecki, and *In re* Warner, quoted above.

Regarding claims 17, 19, and 20, the Applicant respectfully traverses the rejection because the rejection was merely presented again verbatim with no new grounds of rejection being presented and no explanation or rebuttal provided concerning the Applicants' prior response regarding claims 17, 19, and 20. The Examiner's statement that "the rejection still stands due to the rejection of the independent claims 11 and 16" is clearly inappropriate in view of MPEP §707.07(f) and *Ex parte* Schricker, *supra*, and by failing to rebut the Applicant's traversal, the Examiner has failed to establish a *prima facie* case for an obviousness rejection. *In re* Fine, *supra*.

Having presented a rebuttal to the Examiner's rejection, the burden is not on the Applicant to provide evidence at this stage, but rather on the Examiner. *Ex parte* Skinner, *In re* Piasecki, and *In re* Warner, *supra*.

Since the Examiner has produced no such factual basis, withdrawal of this rejection and allowance of claims 17, 19, and 20 is respectfully requested.

Claim Rejections - 35 USC §103

Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (US

Patent No. 6,528,982, hereinafter "Yanagisawa"), and further in view of Jungerman et al. (US Publication No.: 2004/0146097, hereinafter "Jungerman").

Regarding claim 5, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth therein and additionally claims non-obvious combinations thereof.

The Examiner additionally stated that

> "It would be obvious to one skilled in the art to measure the RMS value at the position of the edge as taught by Jungerman et al and incorporating such measurement to Sunter et al's invention to establish sources of the jitter and predict the bit error rate of the communication system so to effectively eliminate jitter found in the signal."

However, the Examiner has not shown or cited a specific section in any of these references that would support the above statement. Thus, no motivation has been presented for a person of ordinary skill in the art to attempt the suggested combination. It is not sufficient that the proposed combination, if feasible, might be beneficial. Rather, it is necessary, as explained in *In re* Sang-Su Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), that there be a specific suggestion in one of the references to make the combination. In *In re* Sang-Su Lee, the Court held that the conclusion of obviousness may not be made from common knowledge and common sense of a person of ordinary skill in the art without any *specific* hint or suggestion in a particular reference.

Inasmuch as the Examiner has not cited in any of these references any such specific hint or suggestion for the combination, the rejection based upon the assumed benefits of the hypothetical combination of Kelkar further in view of Sunter and further in view of Jungerman cannot be maintained, and dependent claim 5 is accordingly believed to be allowable thereover. Allowance thereof is therefore respectfully requested.

Claim Rejections - 35 USC §103

Claim 3 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa"), and further in view of Soma et al. (US Patent No. 6,795,496, hereinafter "Soma").

Regarding claim 3, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth therein and additionally claims non-obvious combinations thereof.

Additionally, the Examiner has not shown or cited a specific section in any of the cited references that would provide motivation for a person of ordinary skill in the art to attempt the suggested combination. It is not sufficient that the proposed combination, if feasible, might be beneficial. Rather, it is necessary, as explained in *In re* Sang-Su Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), that there be a specific suggestion in one of the references to make the combination. In *In re* Sang-Su Lee, the Court held that the conclusion of obviousness may not be made from common knowledge and common sense of a person of ordinary skill in the art without any *specific* hint or suggestion in a particular reference.

Inasmuch as the Examiner has not cited in any of these references any such specific hint or suggestion for the combination, the rejection based upon the assumed benefits of the hypothetical combination of Kelkar in view of Yanagisawa and further in view of Soma cannot be maintained, and dependent claim 3 is accordingly believed to be allowable thereover. Allowance thereof is therefore respectfully requested.

Claims 8 and 13 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa"), further in view of Sunter et al. (US Publication No. 2005/0069031, hereinafter "Sunter"), and further in view of Soma et al. (US Patent No. 6,795,496, hereinafter "Soma").

Regarding claims 8 and 13, these dependent claims depend respectively from independent claims 6 and 11 and are believed to be allowable since they contains all the limitations set forth respectively therein and additionally claim non-obvious combinations thereof.

Additionally, the Examiner has not shown or cited a specific section in any of the cited references that would provide motivation for a person of ordinary skill in the art to attempt the suggested combinations. It is not sufficient that the proposed combinations, if feasible, might be beneficial. Rather, it is necessary, as explained in *In re* Sang-Su Lee, 277

F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), that there be a specific suggestion in one of the references to make the combinations. In *In re* Sang-Su Lee, the Court held that the conclusion of obviousness may not be made from common knowledge and common sense of a person of ordinary skill in the art without any *specific* hint or suggestion in a particular reference.

Inasmuch as the Examiner has not cited in any of these references any such specific hint or suggestion for the combinations, the rejection based upon the assumed benefits of the hypothetical combination of Kelkar in view of Yanagisawa, further in view of Sunter, and further in view of Soma cannot be maintained, and dependent claims 8 and 13 are accordingly believed to be allowable thereover. Allowance thereof is therefore respectfully requested.

Claim 18 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kelkar et al. (US Patent No. 5,663,991, hereinafter "Kelkar") in view of Yanagisawa et al. (US Patent No. 6,528,982, hereinafter "Yanagisawa"), further in view of Sunter et al. (US Publication No. 2005/0069031, hereinafter "Sunter"), further in view of IEEE Design and Test of Computers ("FPGA and CPLD Architectures: A Tutorial", hereinafter "IEEE"), and further in view of Soma et al. (US Patent No. 6,795,496, hereinafter "Soma").

Regarding claim 18, this dependent claim depends from independent claim 16 and is believed to be allowable since it contains all the limitations set forth therein and additionally claims non-obvious combinations thereof.

Additionally, the Examiner has not shown or cited a specific section in any of the cited references that would provide motivation for a person of ordinary skill in the art to attempt the suggested combination. It is not sufficient that the proposed combination, if feasible, might be beneficial. Rather, it is necessary, as explained in *In re* Sang-Su Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), that there be a specific suggestion in one of the references to make the combination. In *In re* Sang-Su Lee, the Court held that the conclusion of obviousness may not be made from common knowledge and common sense of a person of ordinary skill in the art without any *specific* hint or suggestion in a particular reference.

Inasmuch as the Examiner has not cited in any of these references any such specific hint or suggestion for the combination, the rejection based upon the assumed benefits of the hypothetical combination of Kelkar in view of Yanagisawa, further in view of Sunter, further in view of IEEE, and further in view of Soma cannot be maintained, and dependent claim 18 is accordingly believed to be allowable thereover. Allowance thereof is therefore respectfully requested.

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1–20 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 50-0374 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: January 5, 2006